Welcome to the Class

Department of Computing and Information System

Computer Organization & Architecture

Books References

- ***Computer Architecture and Organization***
  Hayes J.P., McGraw-Hill.

- ***Computer organization and design: The hardware/software interface***
  Patterson D.A., Hennessy J.L., Morgan Kaufmann.

- ***Computer Architecture: A Quantitative Approach***
  Patterson D.A., Hennessy J.L., Morgan Kaufmann.

Evolution of computers and computer architecture

First Generation (1940-1950) :: Vacuum Tube

- **ENIAC [1945]:** Designed by Mauchly & Echert, built by US army to calculate trajectories for ballistic shells during World War II. Around 18000 vacuum tubes and 1500 relays were used to build ENIAC, and it was programmed by manually setting switches
- **UNIVAC [1950]:** the first commercial computer
- **John Von Neumann architecture:** Goldstine and Von Neumann took the idea of ENIAC and developed concept of storing a program in the memory. Known as the Von Neumann's architecture and has been the basis for virtually every machine designed since then.

Evolution of computers…….

Features:

- Electron emitting devices
- Data and programs are stored in a single read-write memory
- Memory contents are addressable by location, regardless of the content itself
- Machine language/Assemble language
- Sequential execution

Second Generation (1950-1964) :: Transistors

- William Shockley, John Bardeen, and Walter Brattain invent the transistor that reduce size of computers and improve reliability. Vacuum tubes have been replaced by transistors.
- First operating Systems: handled one program at a time

Continue…..

- On-off switches controlled by electronically.
- High level languages
- Floating point arithmetic

Third Generation (1964-1974) :: Integrated Circuits (IC)

- Microprocessor chips combines thousands of transistors, entire circuit on one computer chip.
- Semiconductor memory
- Multiple computer models with different performance characteristics
- The size of computers has been reduced drastically

Continue…..

1972 – 2010: Fourth Generation

- Combines millions of transistors
- Single-chip processor and the single-board computer emerged
- Creation of the Personal Computer (PC)
- Use of data communications
- Massively parallel machine

2010- : Fifth Generation – Artificial Intelligence

- AI is a reality made possible by using parallel processing and superconductors.
- Leaning to the future, computers will be radically transformed again by quantum computation
- molecular and nano technology.
- 4th Industrial Devices

CPU Organization

- The primary function of the CPU is to execute sequences of instructions, which are stored in memory.

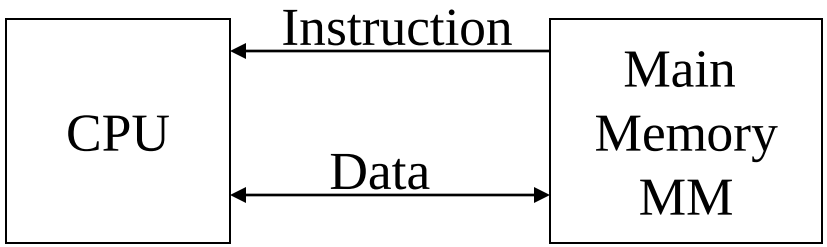
- The execution is carried out in three steps:

1. The CPU transfer instruction and when necessary, their input data (operand) from main memory to registers in the CPU.

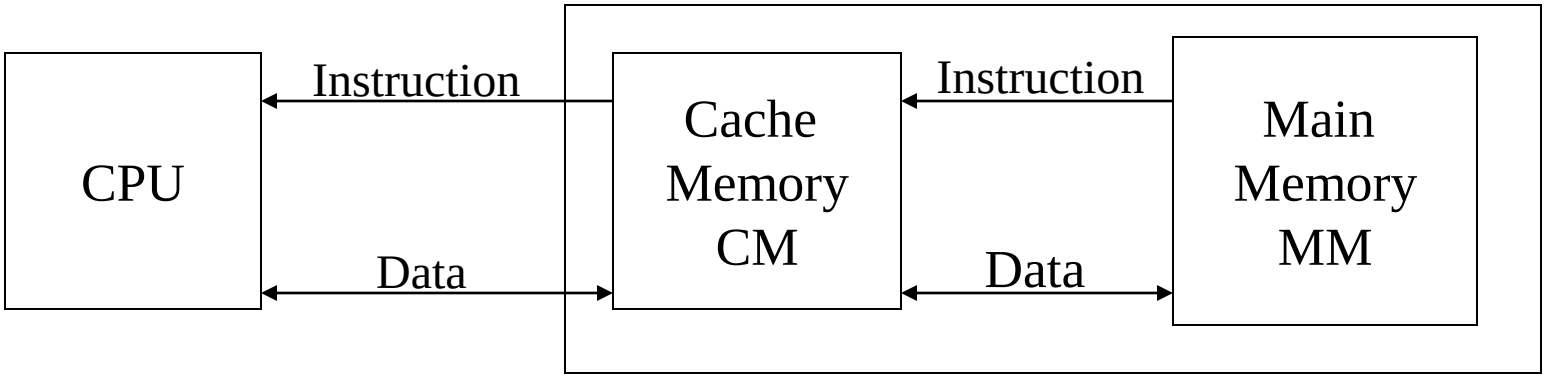
2. The CPU executes the instruction in their stored sequence except when the execution sequence is explicitly altered by a branch instruction.

3. When necessary, the CPU transfers data (results) from the CPU registers to main memory.

External Communication



Processor-memory communication without a cache



Processor-memory communication with a cache

External Communication

- CPU can perform a memory load or store operation from cache in a single clock cycle. On the other hand, the same operations take many clock cycles if they are performed from main memory.

- CPU considers the cache and the main memory as a single, seamless memory space consisting of 2^m addressable storage locations M(0), M(1), …. M(2^m-1).

Communication with IO Devices

- CPU communicates with IO devices in much the same way as it communicates with external memory.
- The IO devices are associated with addressable registers called ***IO ports*** to which the CPU can store a word or from which it can load a word.

Communication with IO Devices

- In some computers, memory locations and IO ports share the same set of addresses, so an address bit pattern that is assigned to memory cannot also be assigned to an IO port, and vice versa. This approach is called **memory–mapped IO.**

- Some computers employ IO instructions that are distinct from memory-referencing instructions. These instructions produce control signals to which IO ports, but not memory locations, respond. This approach is called **IO-mapped IO.**

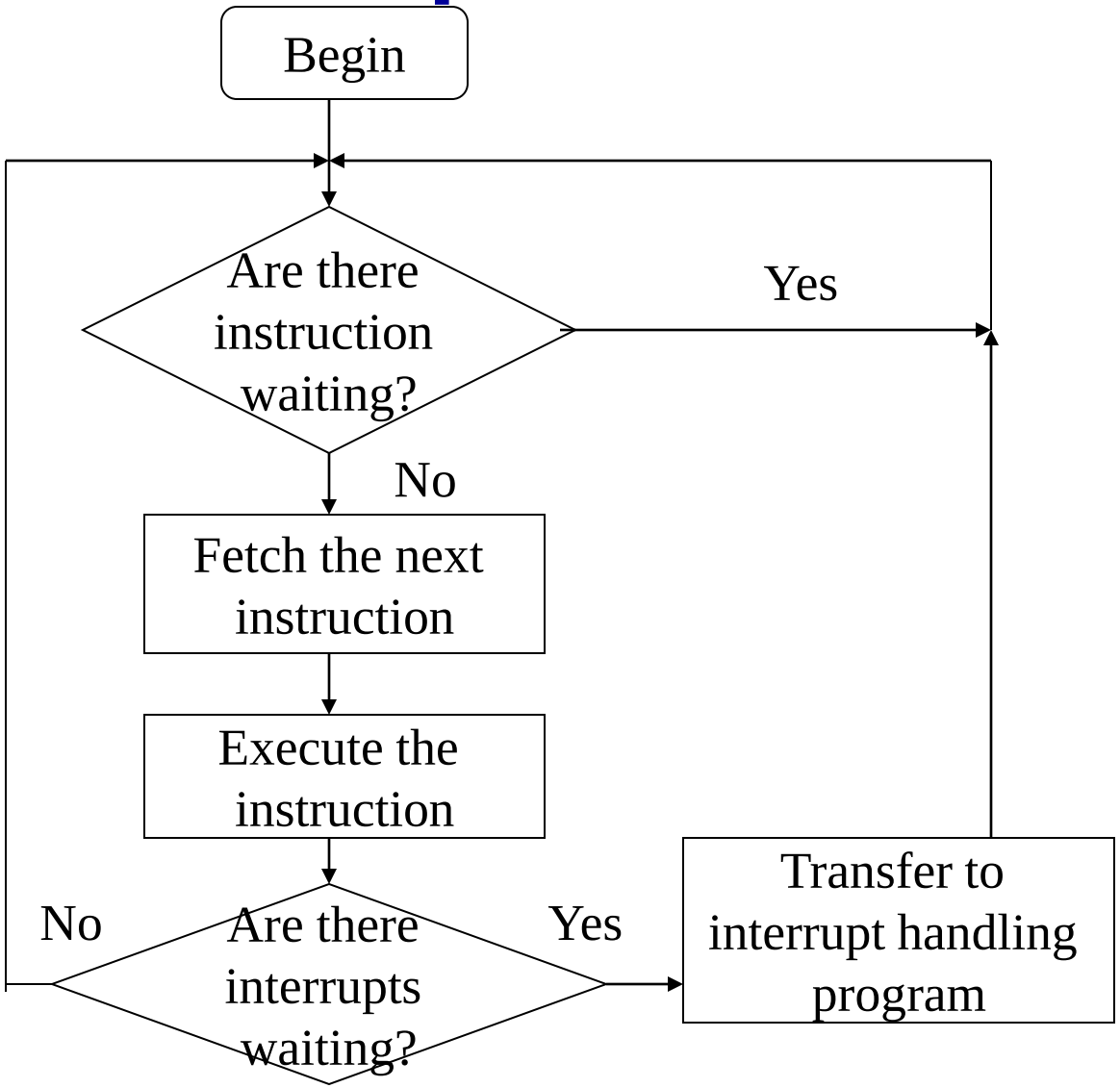
User and Supervisor Programs

- A user or application program handles a specific applications.
- A Supervisor programs manages various routine aspects of the computer system. It is typically part of the computer's operating system.

User and Supervisor Programs

- For normal operation, CPU continuously switches back and forth between user and supervisor programs.
- The requests for supervisor services from the secondary memory and IO devices are known as interrupt.
- In the event of interrupt, the CPU suspends execution of the current program and transfer to an appropriate interrupt handling program.
- CPU frequently check for the presence of interrupt request.

CPU Operation



CPU Operation

- The sequence of operations performed by the CPU in processing an instruction constitutes an **instruction cycle**.

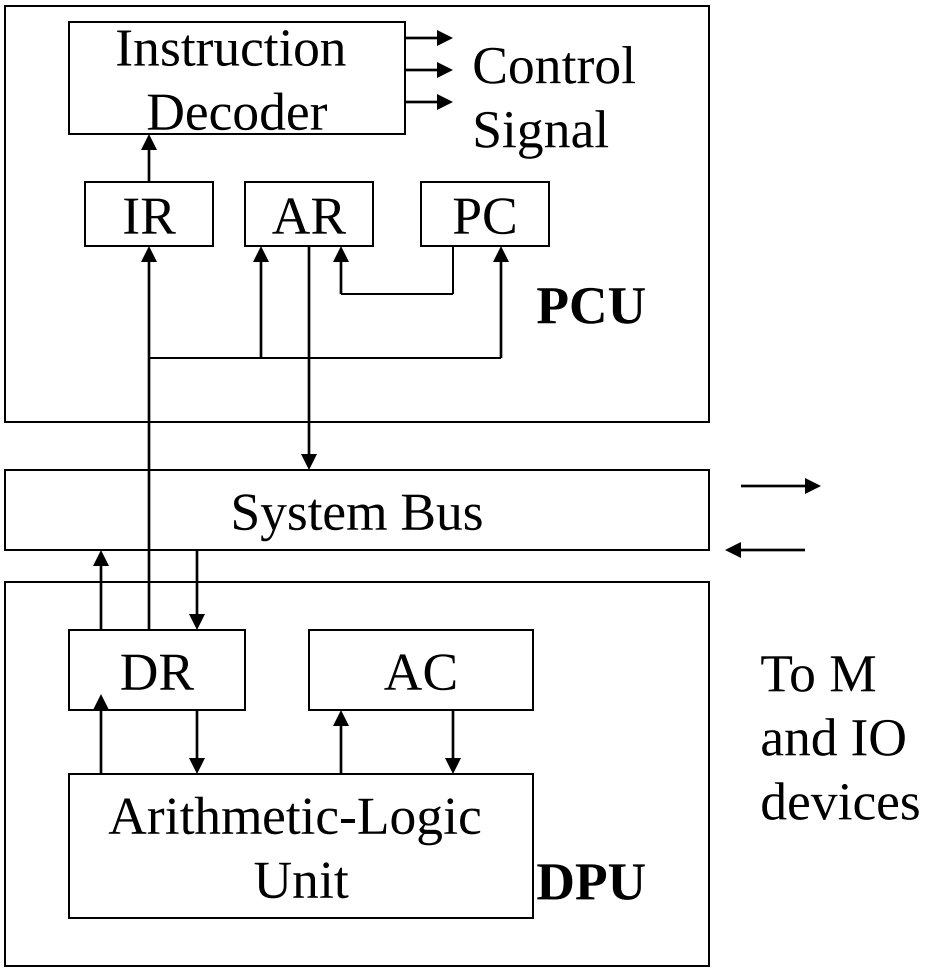
Processing of all instruction generally requires two steps:

1. **Fetch step** - a new instruction is read from the external memory.
2. **Execute step** - The operations specified by the instruction are executed.

CPU Operation

- The actions of the CPU during an instruction cycle are defined by a sequence of micro operations, each of which involves a register transfer operation.
- The time required for the shortest well-defined CPU micro operation is the CPU cycle time or clock period T_{clock}.
- The number of CPU cycles required to process an instruction varies with the instruction type.

Accumulator-based CPU



PCU=Program Control Unit

AR= Address Register

IR=Instruction Register

PC=Program Counter

DPU= Date Processing Unit

AC=Accumulator Register

DR=Data Register

Accumulator-based CPU

- The An instruction that refers to a data word in M contains two parts, an opcode ***op*** and a memory address ***adr*** and ***I=op.adr.***

- Each instruction cycle begins with the instruction fetch operation IR.AR = M (PC), where IR=***op*** and AR=***adr***. Here PC contains the address of the current instruction in the memory.

Accumulator-based CPU

- Instruction that do not reference M do not use AR. Their opcode part specifies the CPU registers to use, as well as the operation to be carried out.

- Once it has placed the opcode of I in IR, the CPU proceeds to decode and execute it. At this point, the CPU can increment PC in order to obtain the address of the next instruction.

Load and Store Operation

- The load instruction transfers a word from the memory location with address ***adr*** to the accumulator.

  AC := M (adr)

- The store instruction transfers a word from AC to M.

  M (adr) : = AC

Any Question???